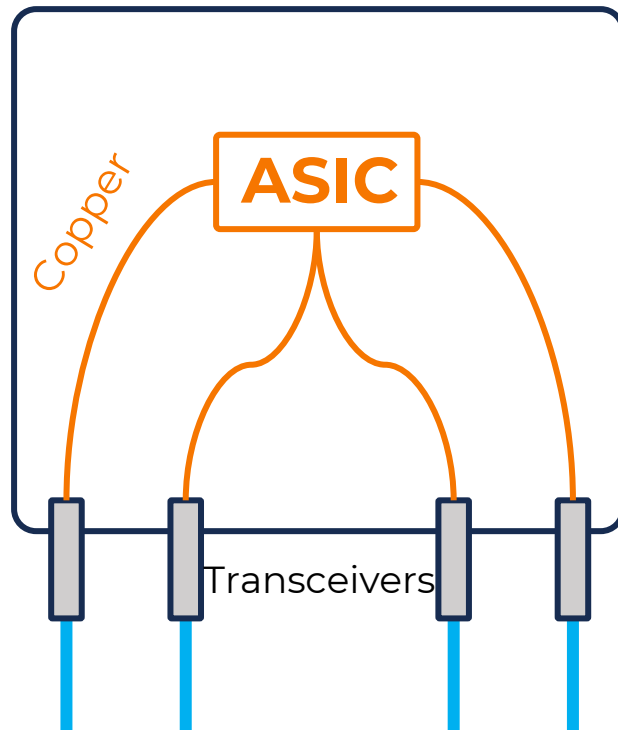




# Using AI-driven wavefront-shaping for scalable optical circuit switching

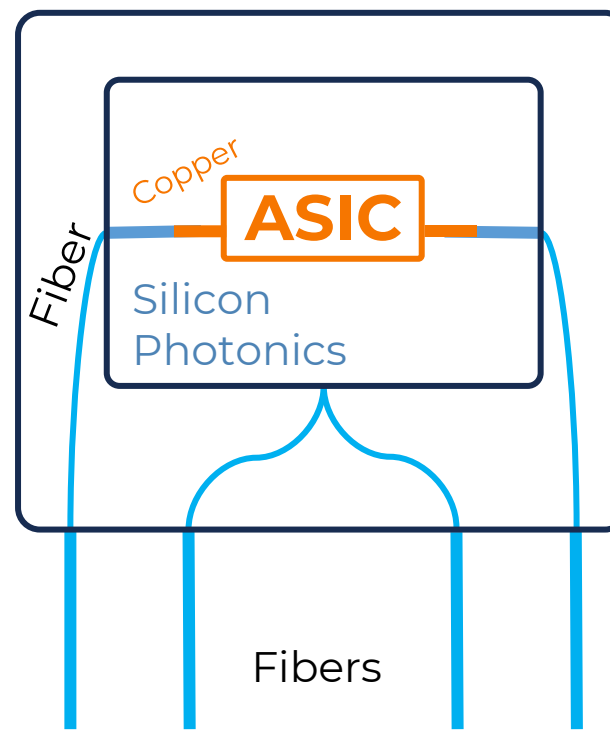
# Photonification of networking

## Pluggable optics



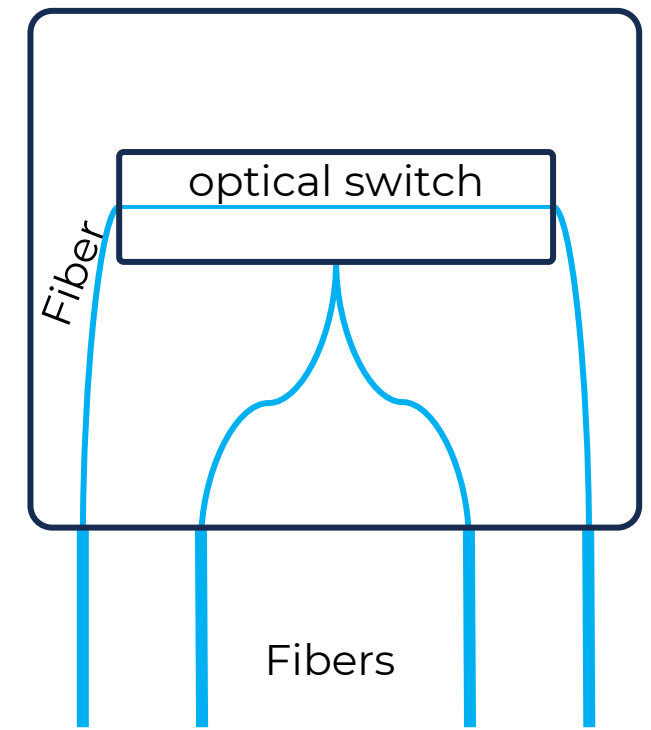
Packet switching latency  
35 pJ/bit (ASIC + copper)

## Co-packaged optics



Packet switching latency  
10 pJ/bit (only ASIC)

## All-optical

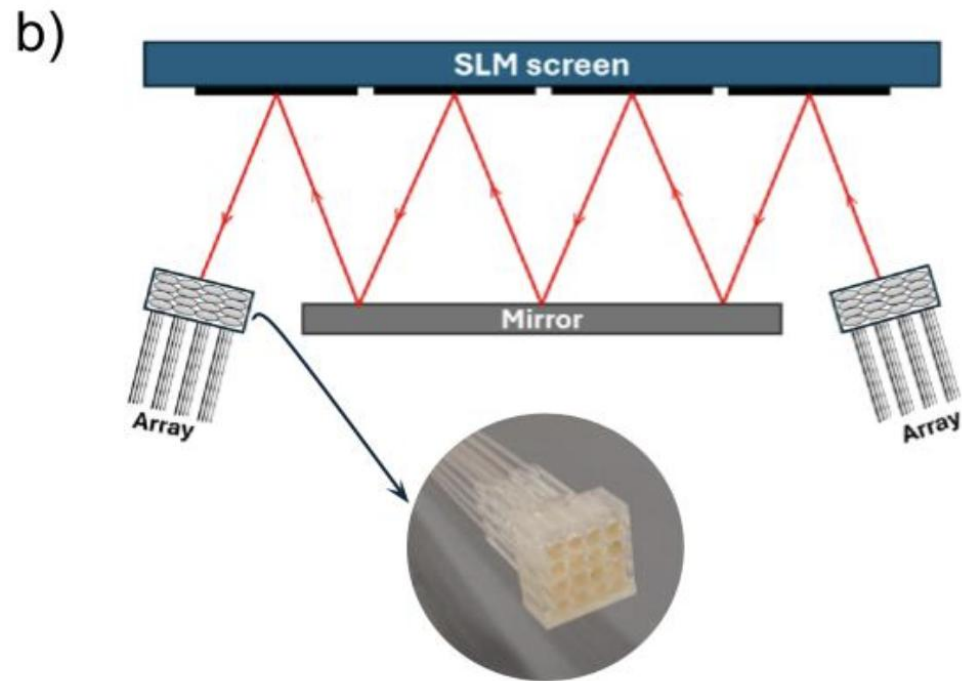
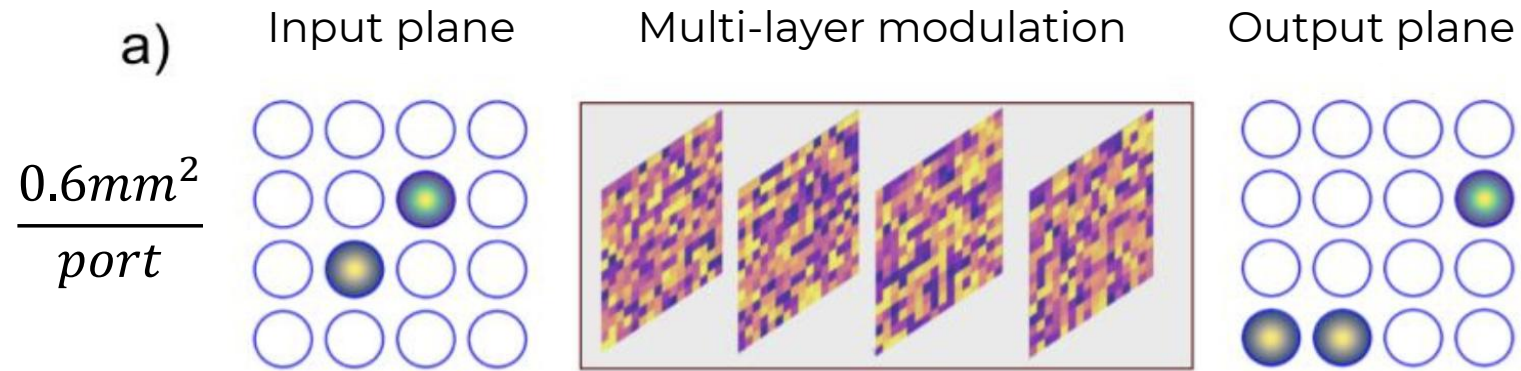


Less than 5 ns time of flight  
Less than 0.2 pJ/bit

Typical energy values given for switch unit (more in system level)

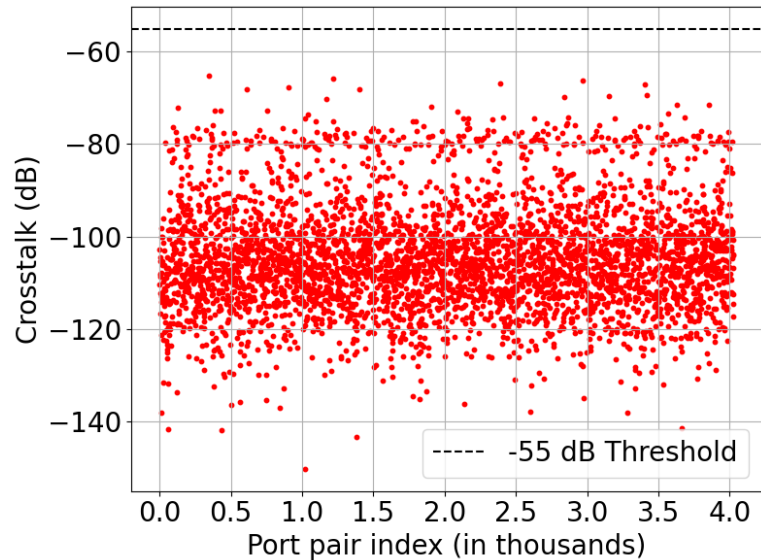
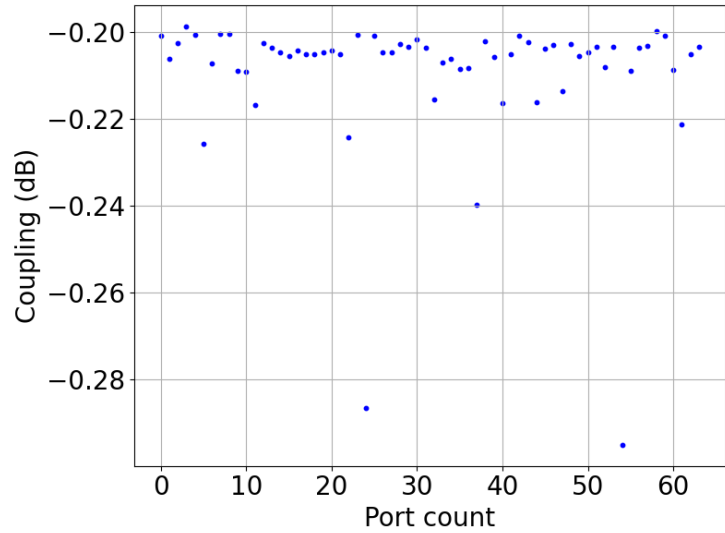


# Multi-layer modulation in zigzag path



# Linear scaling trend between port number and pixel number

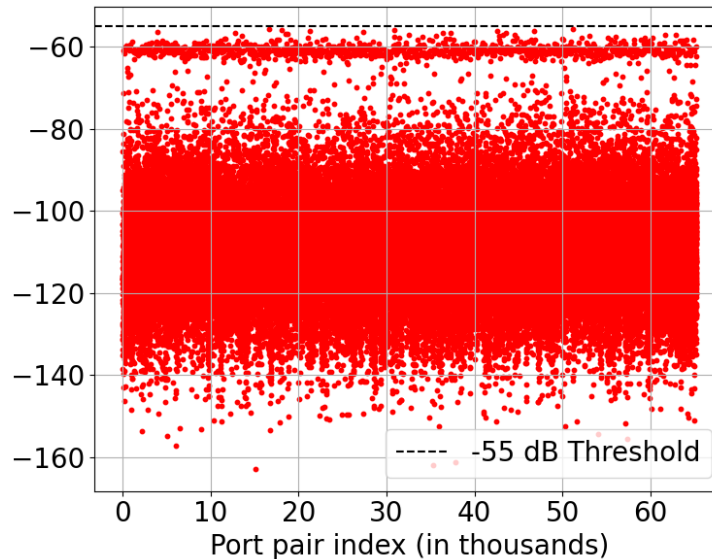
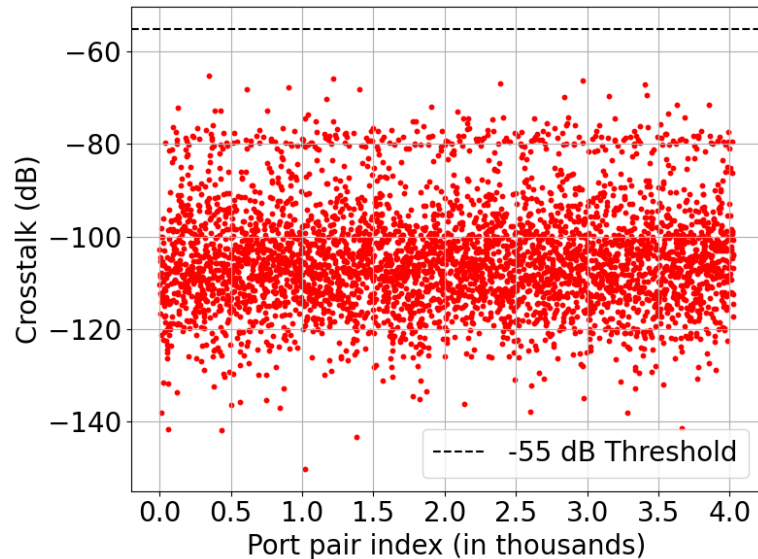
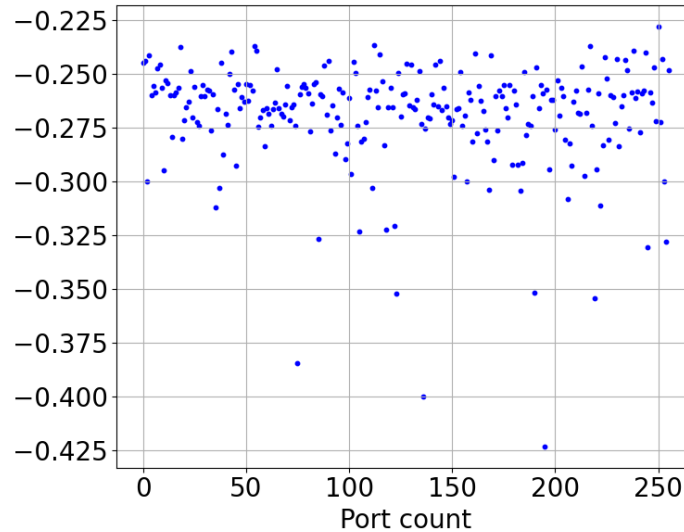
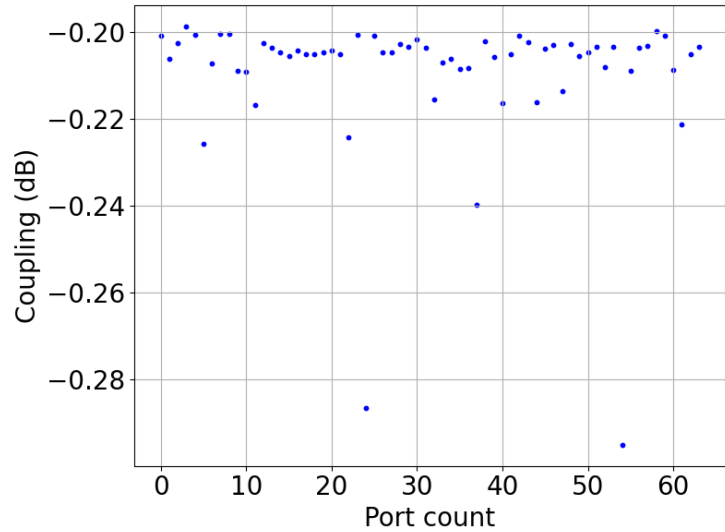
64x64, Normalized Pixel Number: 16384



# Linear scaling trend between port number and pixel number

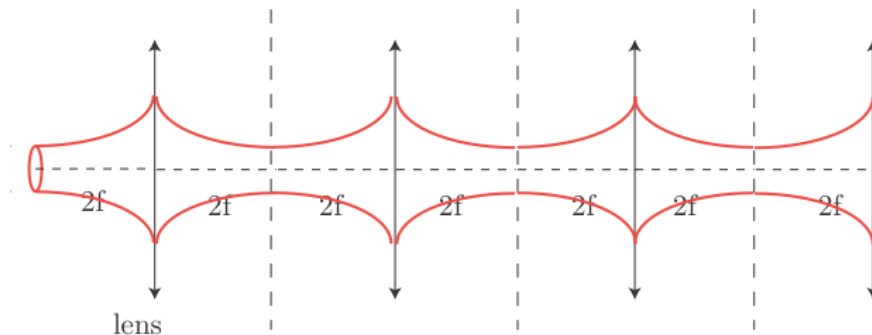
**64x64**, Normalized Pixel Number: 16384

**256x256**, Normalized Pixel Number: 16384

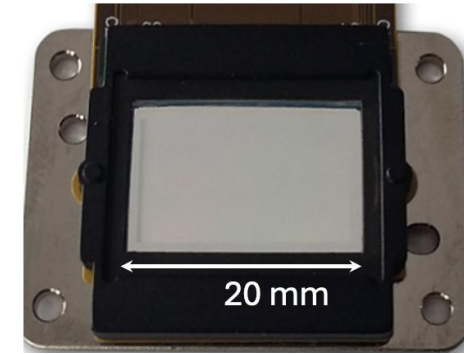
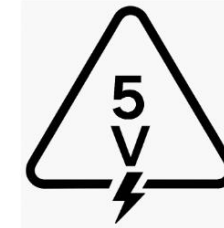
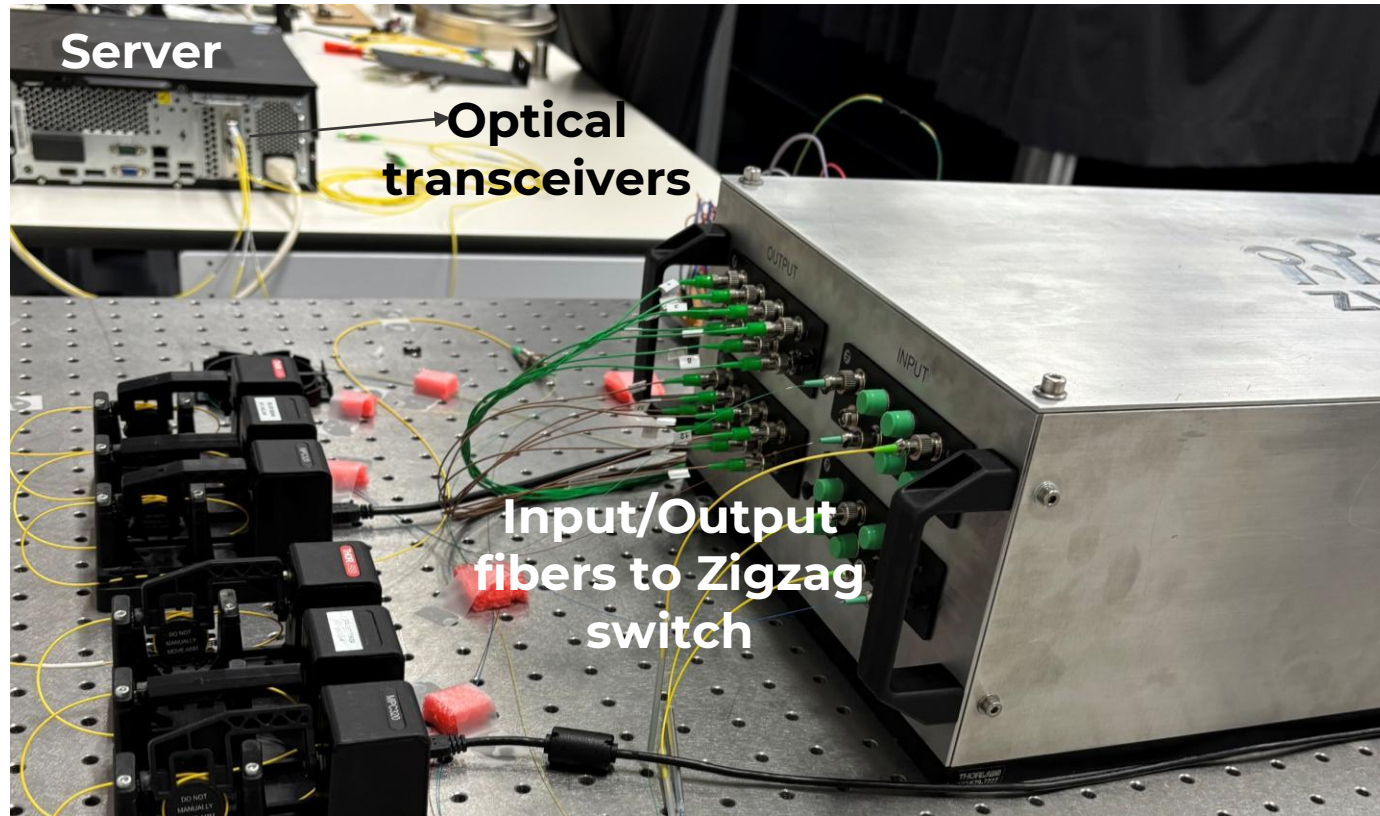


While we increase the port number, we keep the beam width fixed thanks to divergence compensation, leading to linear scaling.

Analogy: Lens Waveguide



# Zigzag PoC with Liquid Crystal on Silicon



1920 x 1200 pixels

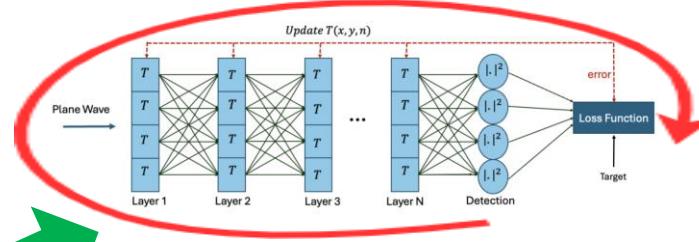
- No moving parts and low voltage drive
- CMOS-compatible back plane: Low cost per port
- Custom efficient SLM: Low loss (< 2 dB)

Design values / Metrics	Zigzag OCS
Loss	5.7 dB
Crosstalk	Less than -55 dB
Port count	16x16

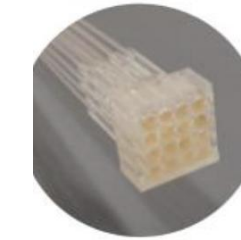
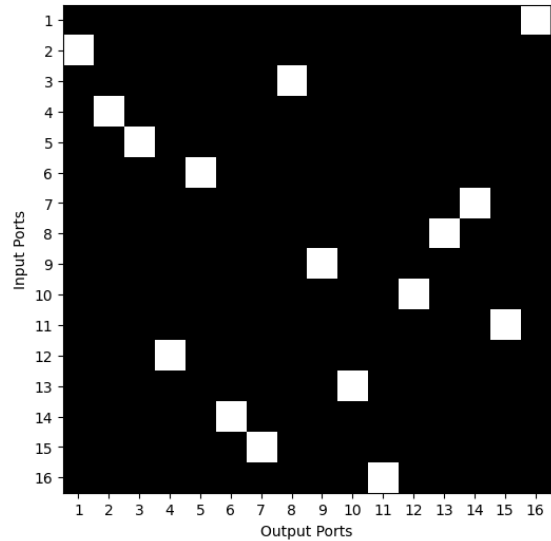


# Driver

## Iterative optimization



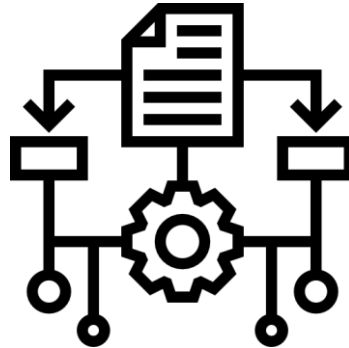
## Connection map



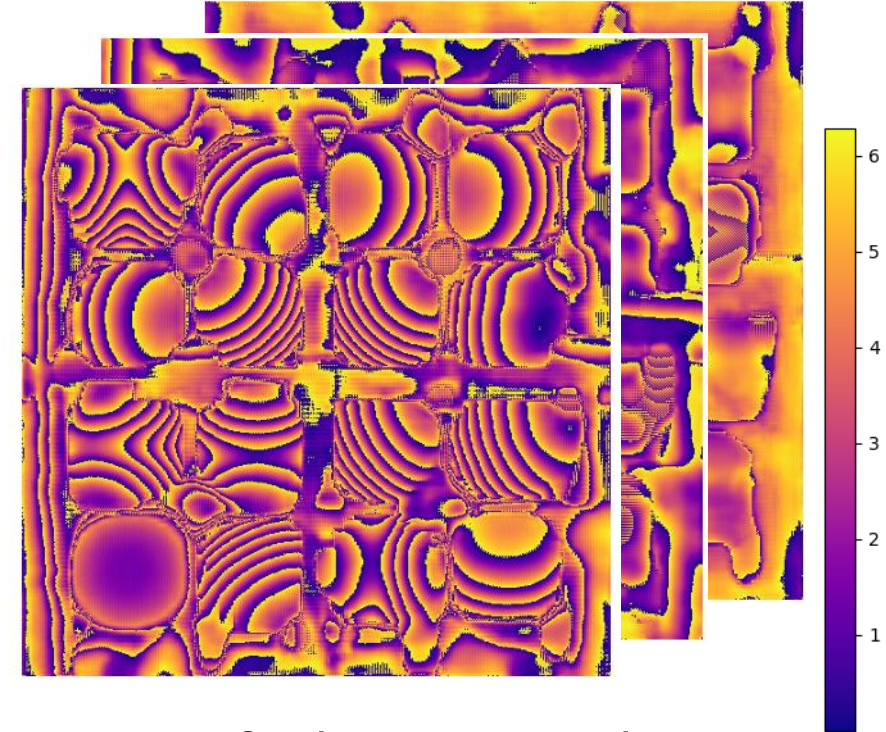
Manufacturing offsets  
embedded in the driver

10 seconds

10 milliseconds



AI-driven Zigzag Algorithm

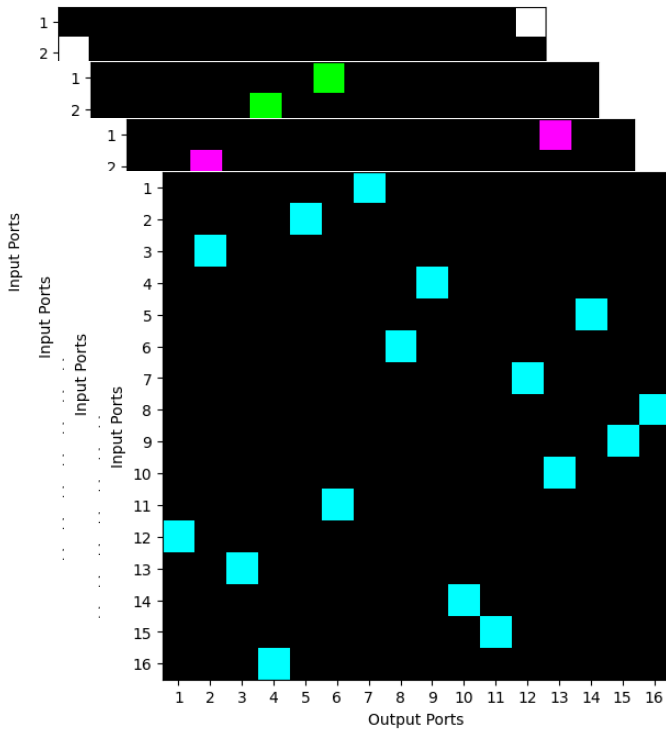


Set of phase masks

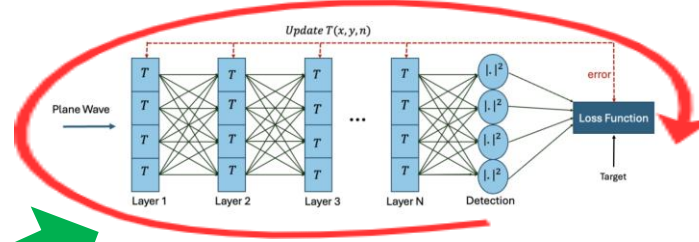
# Driver

Iterative proprietary algorithm

Connection map



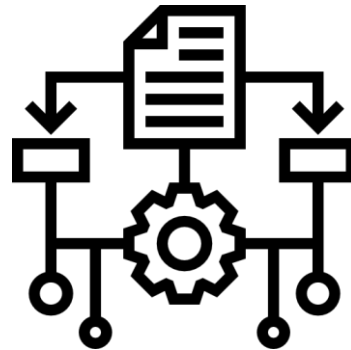
$\lambda$ -selectivity



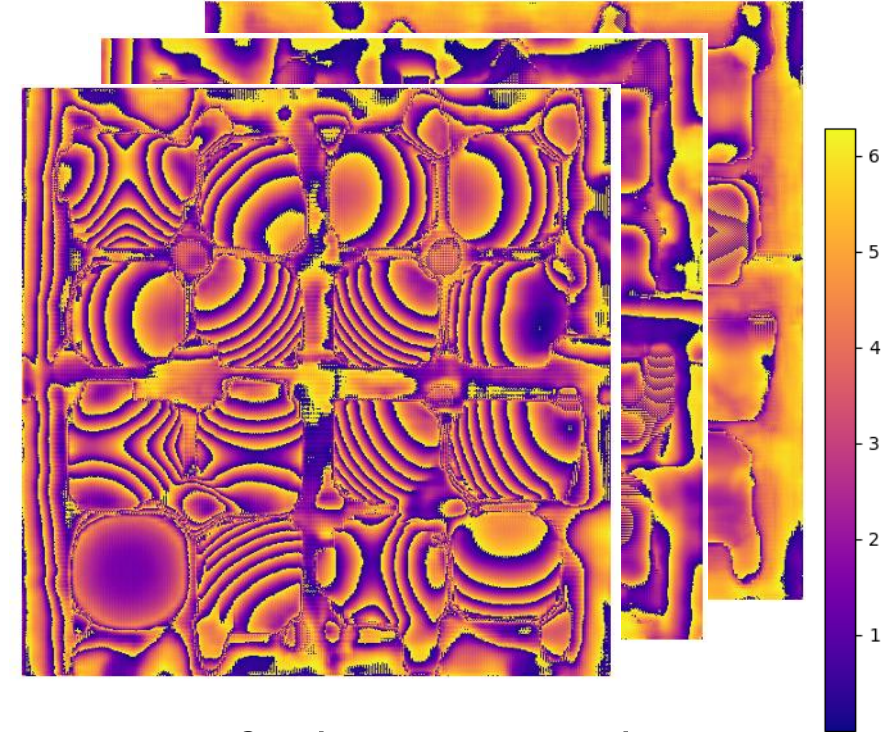
10 seconds

Manufacturing offsets  
embedded in the driver

10 milliseconds



AI-driven proprietary algorithm



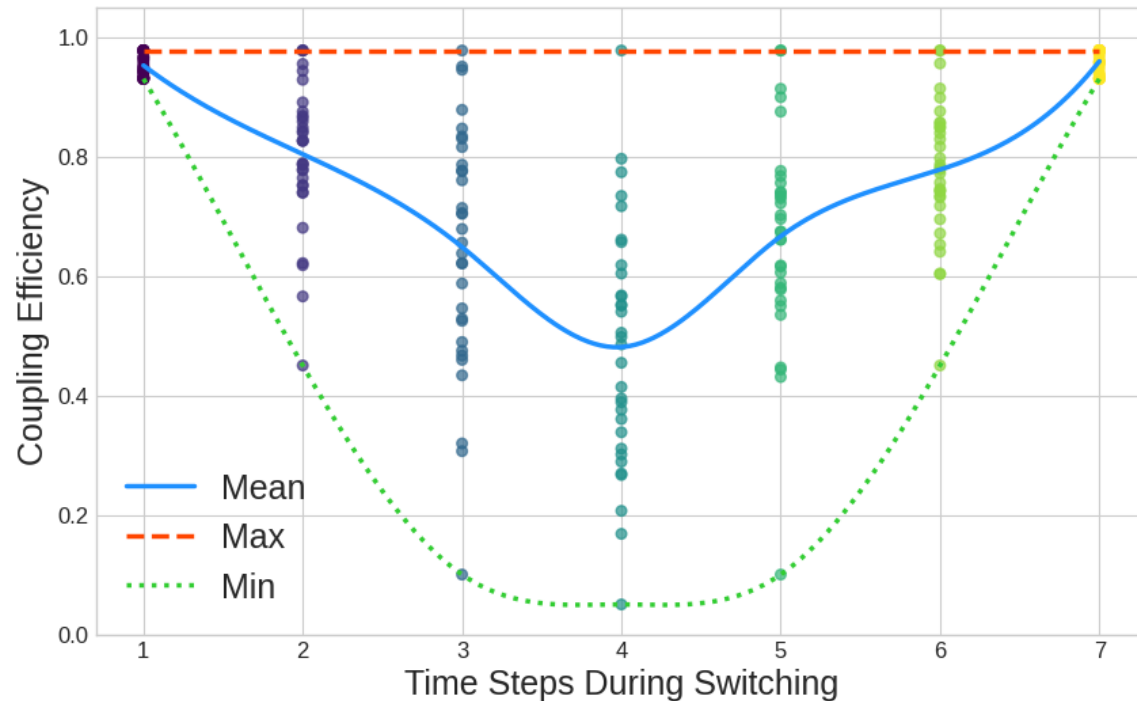
Set of phase masks



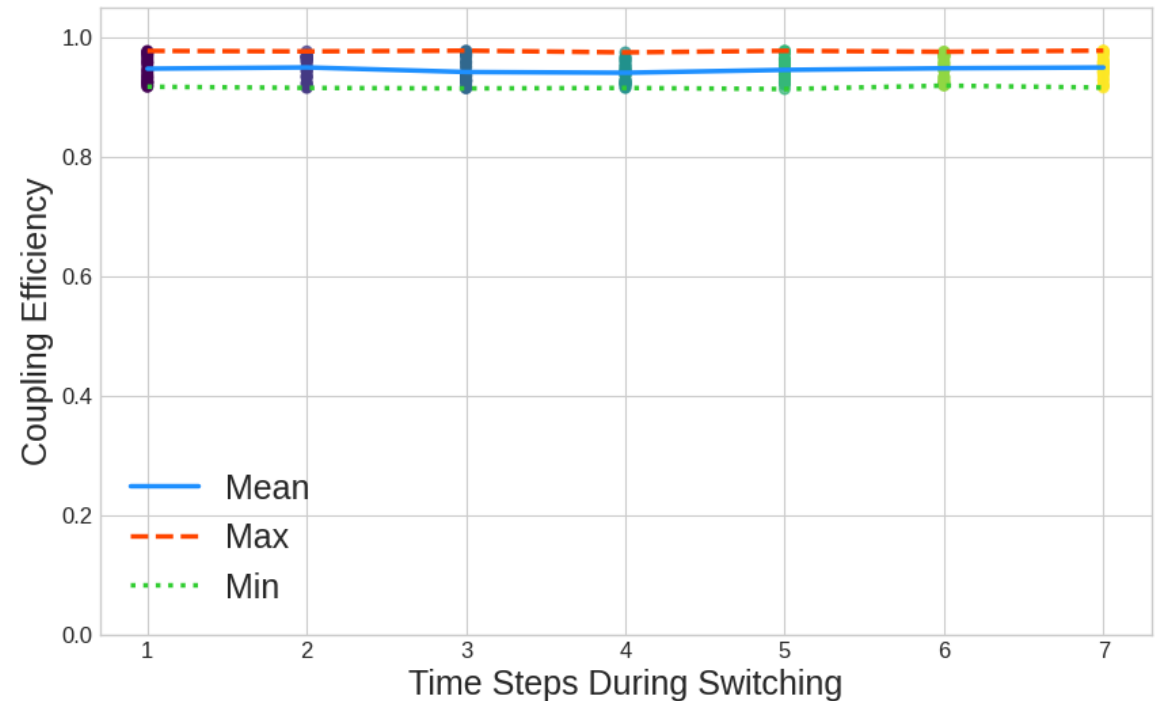
# Nonblocking switching with distributed (multi-layer) modulation

We must ensure that during reconfiguration, the coupling efficiency of the unchanged subset of connections **is not affected**.

Naïve optimization



Our conditioned optimization

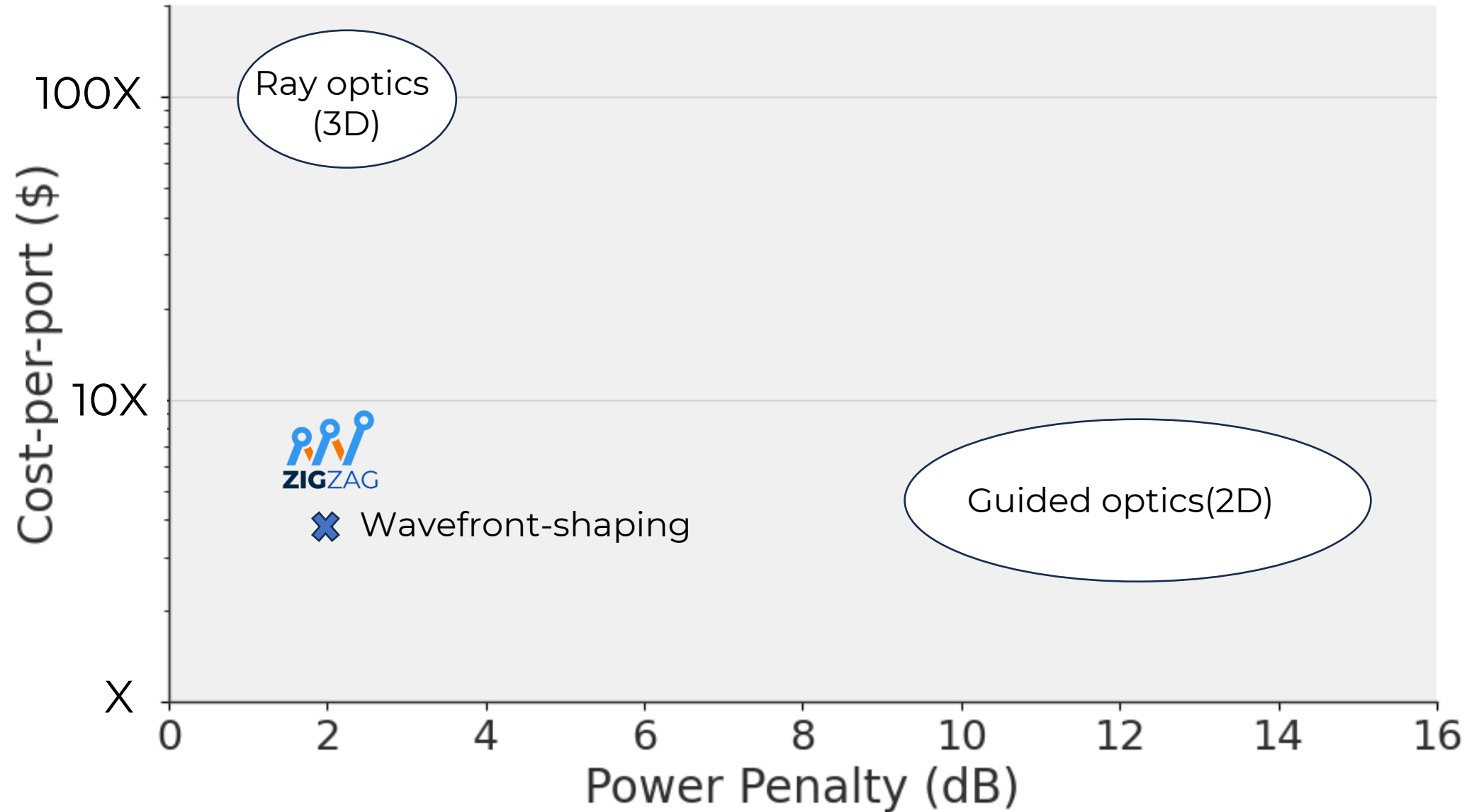


# OCS port economics

Transceiver	Fibers	OCS ports used	Required OCS price multiplier vs. electrical port
DR4 (4 Tx + 4 Rx)	8	8	<b>1/8</b>
FR4 (4λ, duplex)	2	2	<b>1/2</b>
BiDi FR4	1	1	<b>1</b>

**Low \$/port isn't a "nice-to-have," it is a must have for wide adoption**

# OCS Landscape





# Contact us

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